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Engineering at the Nanoscale

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ABSTRACT

An examination of solar cell production through common technique with a comparison to higher efficiency cells. This process produced solar cells with a maximum of power output of 160 μW per cell under ideal lighting conditions and a 1 kΩ load.

Keywords: Nano-scale, Solar Cell, Clean Room, Silicon Wafer, PNP Solar Cell, Physics

1 INTRODUCTION

As the world transitions from fossil fuels to renewable sources, solar cells have emerged as having great potential for large scale energy production. However, before widespread deployment is possible there must be the capability for large scale production. In this lab the characteristics of a monocrystaline solar cell produced by the included method is analyzed and compared to current research to determine if such a method is practical.

2 CREATING THE WAFER

2.1 RCA Clean

The RCA Standard Clean [4] is a multi-step method of wafer preparation that ensures that both organic and non-organic material are removed from the wafer before further processing. One can see the setup for the RCA clean in figure 1

2.1.1 Procedure

1. To remove the organic contaminants on the surface 150 mL of H_2O and 30 mL of NH_4OH were combined in a Petri dish and was heated to 80 °C. Adding this mixture to 15mL of H_2O which will result 6:1:1 $H_2O : NH_4OH : H_2O_2$ and the wafer was placed in this heated mixture for 10 minutes and was then rinsed thoroughly with DI after

2. Normally in an RCA clean the native oxide is removed in a 10:1 $H_2O : HF$, but because of the toxicity of Hydrofluoric Acid this was not done.

3. To remove the ionic contaminants on the surface 180 mL of H_2O and 30 mL of HCl in a Petri dish and it was heated to 80 °C. After this, 30ml of H_2O_2 was added to create a solution of 1:1:6 $HCl : H_2O_2 : H_2O$, the wafer was soaked in this mixture for 10 minutes. After this the wafer was washed in DI water, spun, and blown dry with compressed air.

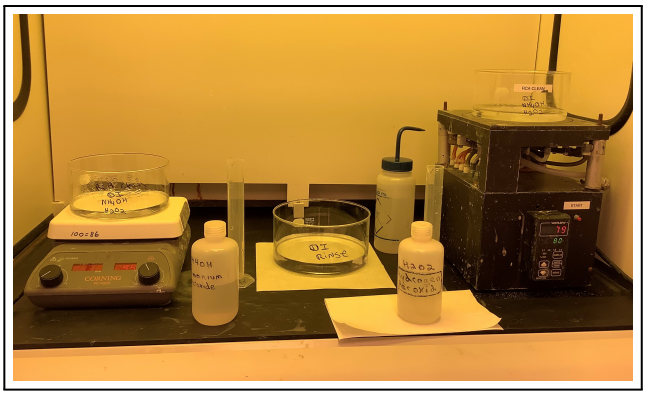

Figure 1. RCA Clean Setup

2.1.2 Oxide Growth

The processed used for this wafer was wet oxidation, which is characterized by the presence of water vapor (steam) in the furnace during the oxidation process. While wet oxidation is generally not used for oxide thicknesses less then 3000 Å due to issues with uniformity, in this situation wet oxidation was selected due to its much higher oxide growth rate (up to 7 times higher then dry) and the need for a 5000+ Å oxide thickness. [1]

1. The furnace was set to 1000 °C and a constant flow of nitrogen at .566l/min was added into the furnace. One can see the insertion to the furnace in figure 2

2. A stream of oxygen at the same flow rate was bubbled through a boiling water bath and also introduced into the furnace. The presence of gaseous H_2O insured a wet oxidation process took place.

3. The silicon wafer was placed in a quartz boat and slowly inserted into a tube furnace set a 1000 °C.
4. After 90 minutes the wafer was removed from the furnace with a theoretical oxide thickness of 5111 Å.
5. The RCA process was repeated as described in 2.1.

Figure 2. Inserting the Cell into the Furance

2.1.3 Oxide thickness

After the conclusion of the wet oxidation process, we used a *Filmetrics F20* to measure the thin film. We did multiple separate recordings to insure that a reasonable value for the oxide thickness was recorded. This was seen in figure 3

A handheld multi meter was then used to measure the resistance of the wafer using the following setup to ensure proper contact as seen in figure 4.

The voltage was also then measured using the four point measuring system for both sides. The results can be seen in table 2.1.3 and the setup in figure 5

First Side		Second Side	
60 uA	60 uA	60 uA	60 uA
-1.461 mV	1.461 mV	-42.93 mV	42.00 mV

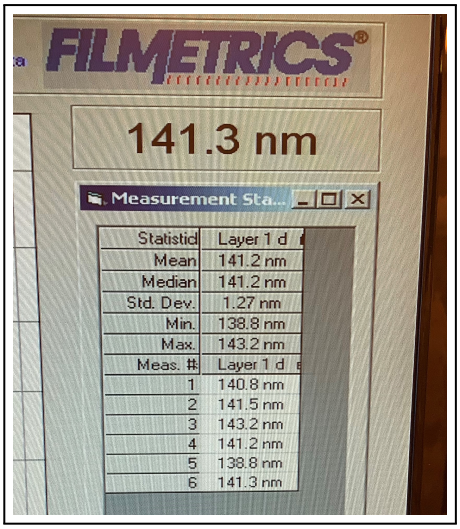

Figure 3. Testing the Wafer Thickness

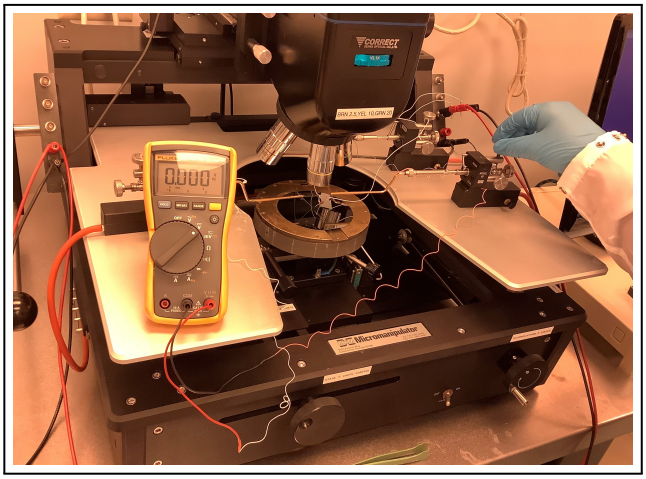

Figure 4. Measuring the Wafer resistance

2.2 Removal of front oxide coating

To remove the oxide coating on the top of the wafer while protecting the oxide coating on the bottom of the wafer we used photoresist to cover the bottom of the wafer and then used a BOE solution to remove any non-covered oxide.

2.2.1 Procedure

1. The wafer was pre-baked on the hot plate at 95 °C for 1 minute.
2. HDMS (hexamethyldisilazane) was spun onto the wafer.
3. *Megaposit SPR 3600* photoresist was spun on the wafer as seen in figure 6
4. The wafer was again backed on the hot plate at 95 °C for 1 minute.

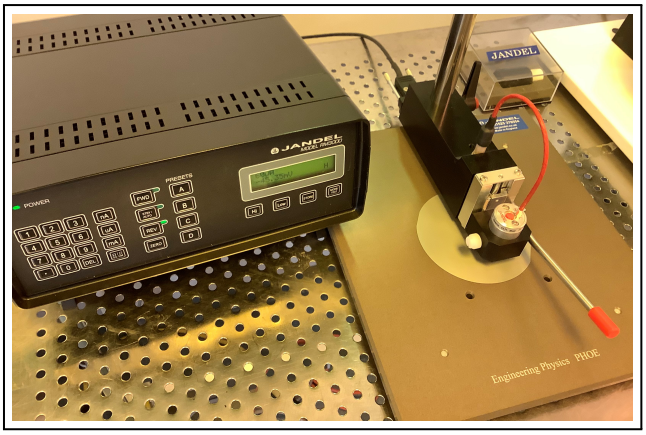

Figure 5. Four Point Measurement

5. Steps 2 and 3 were repeated to form a double layer of photoresist
6. The wafer was post baked at 120 °C for 3 minutes.
7. With the back covered in two layers of photo resist the wafer was submerged into a Buffered Oxide Etch (BOE) solution consisting of 10% HF 2% NH_4F 88% H_2O for 2 minutes.
8. The wafer was washed with DI water.
9. After washing, the wafer was submerged in acetone to remove the photoresist.
10. The wafer was rinsed with DI water, and spun dry.

2.3 Boron Dopeing

To produce the P type on the front of the wafer needed to form an np solar cell, a boron dopant was introduced to the wafer. The chemical process used to implant the boron atoms into the silicon wafer relies on free boron atoms combining with oxygen atoms to form B_2O_3 which reacts with the raw silicon on the front of the wafer to form silicon oxide and borosilicate glass through the following reaction: $2B_2O_3 + 3Si- > 3SiO_2 + 4B$.

2.3.1 Procedure

1. The wafer was placed in a water bath for 30 seconds and then a BOE solution for another 30 seconds.
2. The wafer was then placed in a new water bath for 2 minutes and then rinsed with DI water.
3. Acetone was used to remove the photoresist from the backside of the wafer.
4. Methanol was then used remove the acetone.
5. The wafer was rinsed with DI water to remove the acetone and spun dry.

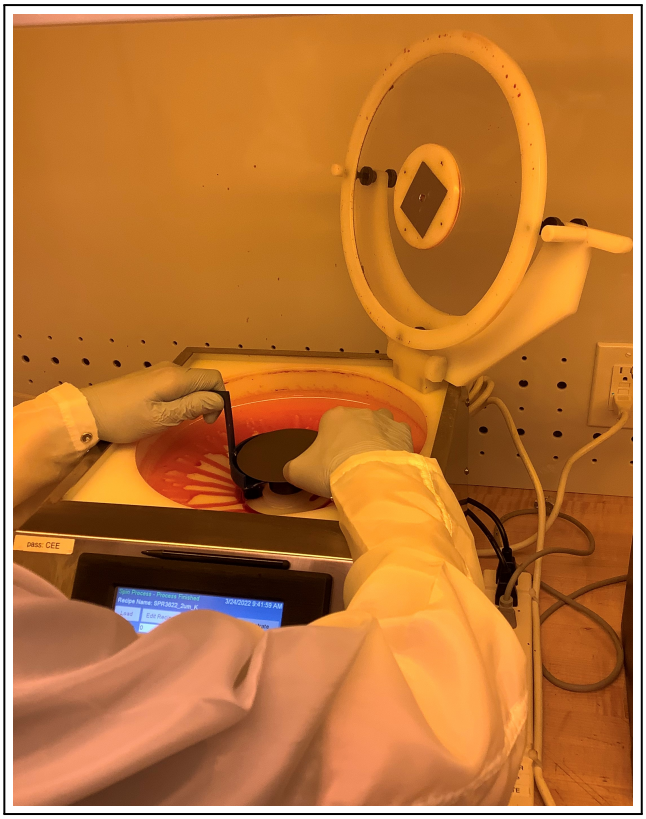

Figure 6. Applying Photo Resist to the Cell

6. The wafer was loaded into the wafer boat.
7. After the doping process was complete in the furnace the wafer was removed.

2.4 Borosilicate Removal

To create contacts to allow the solar panel to be tapped for energy use the insulating Borosilicate glass (BSG) layer and the Silicon Oxide layer must be removed. The Silicon oxide was removed using a BOE etch, while the BSG was removed using a glass etch.

2.4.1 Procedure

1. To remove the oxide coating the wafer was placed in a BOE etch solution for 30 seconds, and then rinsed with DI water.
2. To remove the glass the wafer was placed in a 1:1 $H_2SO_4 : HNO_3$ glass etch for 20 minutes and then rinsed with DI water.
3. The electrical properties were measured using a 4 point probe and multi-meters.

2.5 Photo-lithography

In this section photo-resist was spun onto a silicon wafer using a spinner along with projecting images and embossing them to the wafer with the photo resist allowing the creation of the final pattern for the wafer.

2.5.1 Procedure

1. Photoresist Spin

   After the oxidation a photosensitive material was placed onto the wafer therefore allowing mask pattern in be generated on the material.

   Being temperature sensitive the photoresit can be poured into beakers after beginning warmed to room temperature.

   The thickness of the film obtained depends on the resist's properties and the spin speed. With a given film thickness one can determine the spin speed from the manufacture's graph.

   A smooth resist coating is obtained by ramping up the check to speed in several stages which are programmed in the spinner

   (a) The chuck is ramped up to 2000 RPM in one second and maintains rotation for ten seconds

   (b) That rotation is maintained for 40 seconds

   (c) Wafer decelerates to zero in one second

2. Soft bake

   The soft bake is a drying process which is used to remove excess solvent, and this also stabilizes the resist film at room temperature. There are four effect of removing solvent from photo-resist film.

   (a) The film thickness is reduced

   (b) Post exposure bake and development properties are changed

   (c) Adhesion is improved

   (d) The film becomes less tacky and thus less susceptible to particulate contamination

   To complete the soft bake procedure one must simply place the wafer on the hot place for 1 minute at 90 degrees Celsius

3. Exposure

   The wafer, ready for exposure, was placed in the *Suss Microtec* mask aligner resulting in an oxidized wafer with exposed photoresist wherever the mask was clear.

4. Development

   After exposure the photo-resist must be developed, with like most photo-resist an aqueous base.

   These characteristics of the resist-developer interaction determine the shape of the photo-resist profile and the line-width control. After the development process is completed a clear pattern was observed as seen in figure 7

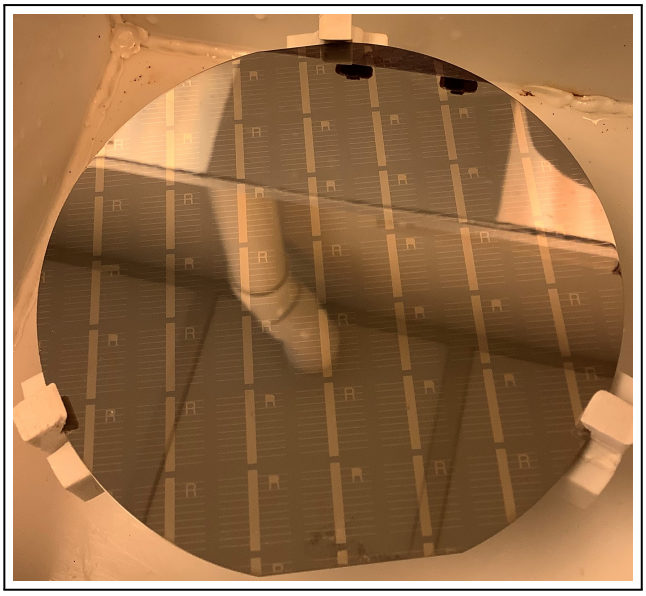

Figure 7. Photo Showing the Pattern That was put onto the wafer

5. Post-bake

   The post-bake process us used to harden the final resist so that it can withstand the harsh environments of etching. This was completed by simply baking on hotplate for 1 minute at 115 degrees Celsius. This makes the image more stable.

   The resist was then developing using the *Shipley Microposit 351* developer diluted with DI water in a ratio of 1:3.

6. Lithography Process Completed

   The first lithography process is now completed and the pattern is masked in a resist covered wafer. The wafer can now be placed on the micromanipulator stage and the CCD camera plus the EPIX software was used to capture images as seen in figure 8 and 9

2.6 Metal Deposition

To allow electricity to flow out of the cell conductive contacts must be added to each solar cell. Because aluminum bonds well to silicon and has a closer work function to that of pure silicon, aluminum was added directly to the silicon surface. To make soldering easier a layer of copper was then deposited onto the wafer. Both a sputtering process and a e-beam evaporation process were used to allow for a pipelineing effect where two wafers could be worked on at once. Since a lift of method of extra metal was used the metal layers could not exceed $1/2$ the thickness of the photoresist.

2.7 Procedure

1. The water to the sputtering system was turned on. The sputtering machine can be seen in figure 10

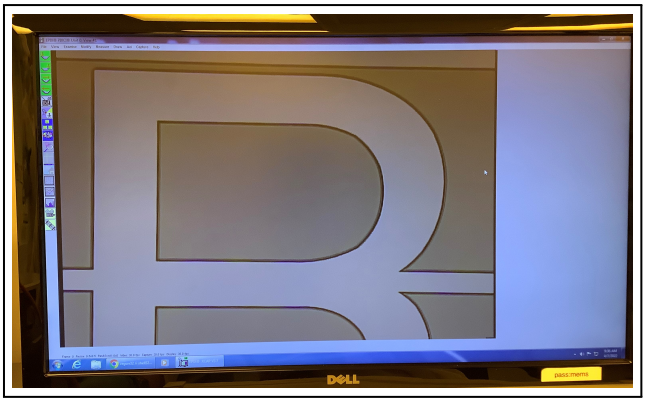

Figure 8. Wafer Under the Microscope showcasing the R in the pattern

Figure 9. Wafer Under the Microscope showcasing the defects

2. The wafer was placed on the substrate holder and slid onto the transfer arm in the load lock and the door was closed.
3. To protect the vacuum pump the turboprop valve was closed.
4. The rough pump valve for the load luck was opened.
5. The load lock was allowed to reach the 10mTorr range.
6. The valve to the rough pump was closed.
7. Now at a reduced pressure, the vacuum pump was run.
8. The gate valve was opened, allowing the transfer of the substrate into the sputtering chamber
9. The substrate holder was slid in, and the holder was locked in place a quarter turn around.

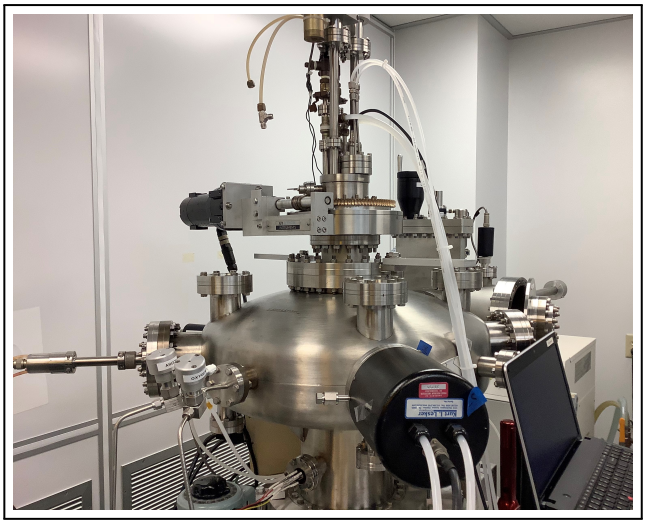

Figure 10. Plasma Sputtering Machine

10. The transfer arm was removed from the chamber and the gate valve was closed.
11. To align the components the substrate was rotate until it was facing the the aluminum gun.
12. The crystal monitor thickness was zeroed
13. At this point pure Argon was introduced into the chamber at a rate of 60 SCCM (Standard Cubic Centimeters per Minute).
14. To initiate the plasma the power supply was set to 300W and started. The plasma glow was then observed as seen in figure 11
15. When the crystal monitor recorded the correct crystal thickness the power-supply was shut off.
16. The Aragon flow was turned off and the sub-started was rotated to the load and unload position
17. The gate valve was opened and the substrate and holder was removed.
18. The arm was then removed from the system, the gate valve closed, and the rough pump door closed.
19. To prevent over pressurization of the load lock chamber the lock on the door was loosened.
20. The load lock was vented until the pressure difference was small enough that the door could be opened.
21. The sample was removed from the machine.

2.8 E Beam Evaporation

Using the E Beam evaporation machine was used to deposit copper onto the device allowing for soldering to take place. The E Beam Machine can be seen in figure 12

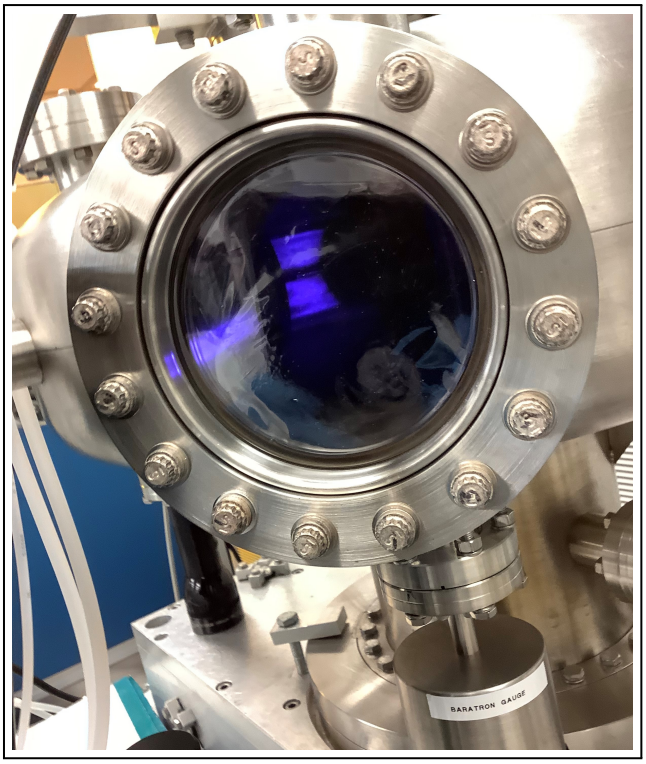

Figure 11. Glowing Plasma in the Sputtering Machine

Figure 12. E-Beam Machine

2.9 Lift off Al and Cu

Liftoff is a method of masking a patterned film. Placing photo-resist down prior to deposition of the desired film the process, relying upon a solvent attacking the underlying photo resist and gentling lifting away any metal lying above the photo resist, will begin. The metal remaining in places where the photo resist is absent will leave the pattern on the wafer.

Liftoff relying on the solvent removing the photo resist is limited on the thickness of the film that can be removed. The photo-resist thickness must be larger than the deposited film, that way small regions can gain access to the photo resist. A good rule that one should follow is that the photo-resist should be twice as thick as the deposited film.

2.9.1 Procedure

1. The sonicator was filled with DI water until nearly full.
2. The Pyrex dish was filled $\frac{1}{4}$ of the way full with acetone.
3. The Pyrex was placed in the sonicator and then the wafer was placed in the pyrex dish and the sonicator was turned on as seen in figure 13
4. After 30 second the wafer was removed and the excess thin film was removed with a cotton swab.
5. The wafer was then removed after all of the metal in the unwanted regions was removed.
6. The wafer was then rinsed with methanol and DI water, and then spun dry.
7. Images were captured of the wafer.

2.10 Dicing

Since the wafer contains many separate solar cells on one wafer, it is necessary to split the wafer into individual components before packaging. To do so a water cooled wafer saw was used. The wafer saw was not used to cut completely through the wafer, but instead to create high stress troughs to facilitate snapping individual cells of.

2.10.1 Procedure

1. The wafer saw was turned on and the wafer seated on the cut bed.
2. To ensure that the cuts made were even and in the right locations the wafer was aligned relative to the wafer saw. As seen in figure 14

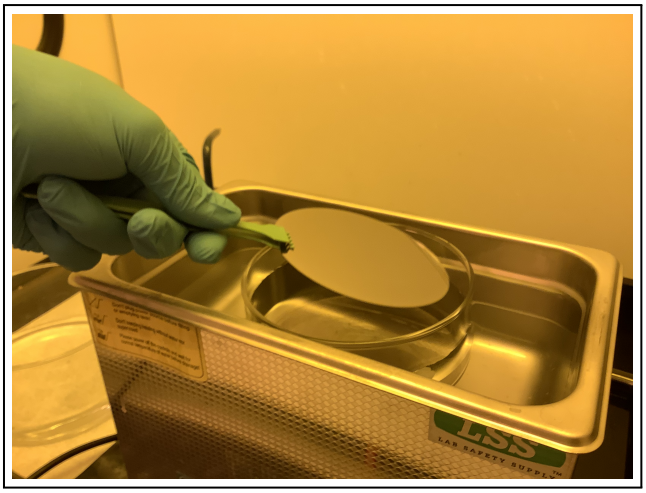

Figure 13. Wafer in the Ultrasonic Bath

3. Both the vertical and horizontal size of the wafers were input into the saw.
4. The horizontal cuts were made first, the wafer was rotated exactly 90° and the vertical cuts were made.
5. The sliced wafer was then run through the RCA clean as described in section 2.1. Any pieces that disconnected from the main wafer were washed individually.

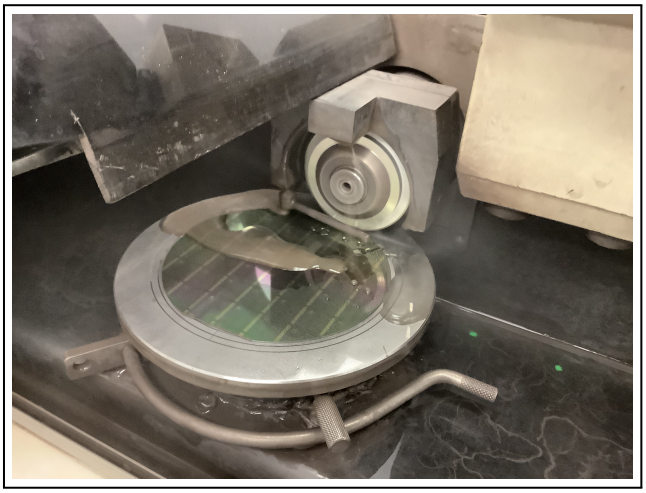

Figure 14. Dicing the Wafer

2.11 Electroplating

To improve the solder joints used in the packaging step the solar cells were electroplated with copper solution. The additional copper significantly reduced the difficulty of soldering and improved the electrical conductivity of the soldering joints. Because of these benefits, this step is strongly recommended even if it is possible to solder onto the copper deposited with the e-beam setup.

1. The individual cells were masked with electrical tape over the non copper contact areas and attached to a copper cathode.
2. A .5 mol solution of copper sulfate was prepared by adding Copper Sulfate crystals to DI water.
3. The copper sulfate solution was poured into a the borosillicate glass graduated cylinder along with the copper cathode with the solar cells attached and a copper anode made out of the bent piece.
4. A voltage of 5 volts was connected across the anode and cathode without a current limit.
5. After 10 minutes the cells were removed and flipped around, as to allow the side previously against the cathode to become coated in copper.
6. The cells were placed back into the solution for an additional 10 minutes with this arrangement.
7. Once removed the cells were thoroughly washed in DI water.

2.12 Packaging

To ensure the safety of the cell during testing and to provide easy contact points to the cell each solar cell was in-cased in a 3d printed holder using a glass slide and liquid super glue.

Copper wires were soldered onto both the front and back copper contact pads using unleaded solder and a soldering iron temperature 345°C.

The cell was placed on top of a glass side mounted on a 3d printed holder.

The copper wires were arranged to lead out of the holder without touching, and the top of the holder was tightly fitted to the other portion.

A liberal coating of high viscosity super glue was poured onto the solar cell until the entire cell was covered.

The solar cell assembly was placed in a secure location without disturbance for 24 hours to fully cure.

3 TESTING THE WAFERS

Since the importance of solar cells is directly dependent on their efficiency at turning natural light into energy, the testing procedure was designed to test energy capture along with the device characteristics. For energy capture an artificial light source was used, and to characterize the solar cells component behavior an oscilloscope and function generator were used.

3.1 Power Generation

While solar cells are normally tested at frequencies that corresponds with the peaks in the available power from the sun at earths crust (275, 390, and 430 nw)[3]. To ensure repeatability without the use of speciality gear, the LED light of a Samsung Galaxy Note 9 at full power was used as the light source. The power measurement was conducted using both an amp meter and a ohm meter to simplify calculations.

1. The one of the two leads of the solar cell package was connected to a 1kΩ resister, and the other lead was connected to a amp meter.
2. The end of the resister was connected to the amp meter to close the circuit, and a voltage meter was connected over the resister.
3. The LED (.2W rating) of the the smartphone was placed directly on the top of the solar cell and the voltage and current was measured.
4. The readings on the amp meter and voltage meter were multiplied together to find the power produced by the solar cell.
5. Multiple solar cells were tested in the manner and the results averaged together. We measured a power output of the solar cell to be 160 $\pm 5\mu$W in this configuration for an efficiency of .

3.2 Testing Procedure

1. Give the Solar cells behave as a diode one can use a very similar procedure to obtaining a diode's transfer function with a solar cell.
2. The following circuit was constructed as seen in figure. 15

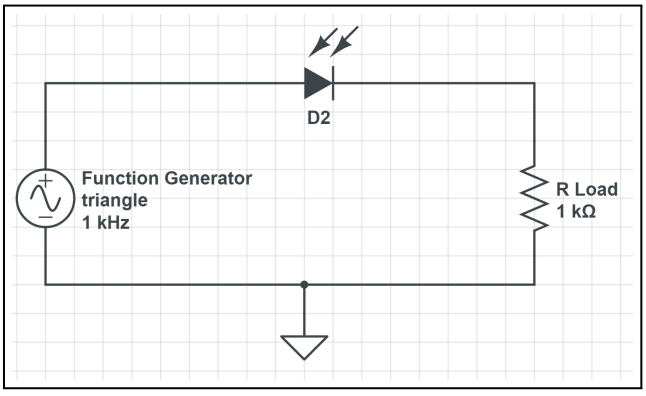

Figure 15. Circuit Diagram for the Transfer Function

3. The voltage source used was a function generator. By setting the function generator to a ramp function one can do a DC Sweep of the diode.
4. One can put scope probes onto the input and the output. By default the scope will then show a transient response of the circuit. However we want to see the transfer function of the circuit as described by equation 1 where m is the slope of the transfer function and where b is the offset caused by the the diode emitting current. By looking at this one can clearly see the "generation" of power from the sun.

$$V_{in} * m + b = V_{out} \tag{1}$$

To get this transfer function one can simply use the X Y mode of the scope. As outlined below:

Transfer Function Procedure

Measure V_{in} using channel 1 and V_{out} with channel 2. Chanel 1 will also be referred to as **X** and Channel 2 will also be referred to as **Y**.

The menu button in the triggering area of the scope was selected and the course was chosen to be Channel 1.

The **ACQUIRE** button was pressed which allows one to select the **X Y Display**. Selecting this will give one a trigged X Y view of the 2 channels.

Using the High Resolution mode on the scope one will resolve the fuzziness.

The channels were zeroed and the volts per division were adjusted to fill the entire scope screen.

Using the delta measurements to the side one can obtain the transfer function slope.

After this procedure was completed scope outputs were obtained with verify the functionality of the solar cell. One can see these scope outputs at the end of the document that are enlarged to show detail.

4 CONCLUSION

The efficiency of the solar cells produced using this lab procedure was approximately 0.08 % when measured using the test setup described above. This efficiency does not even compare to the the 20%+ achieved in more modern designs using textured surfaces and other advanced design techniques [2]. There are several factors that may have contributed to this much lower then expected efficiency including:

1. The fact that not all light emitted by the LED hit the solar cell. Since the LED was extremely wide angle, even when placed directly against the solar cell, some light was lost to the sides of the phone.

2. Some light reflected off of the wafer instead of being absorbed.

3. The degree to which the load resistance used deviates from the ideal load resistance for maximum power.

4. Most of the efficiencies issues were likely caused by the wavelength of light emitted by the phone LED not matching up with the frequency absorbed by the solar cell.

That said, for the procedure described in this document, the approximate time commitment from amateurs is only 15 hours in lab to complete from monocrystaline silicon wafer to tested product. All steps listed were either done in a level 6 clean room or a regular electrical testing environment. Considering this, the procedure is more accessible for replication. For a device created under these conditions to produce a notifiable and significant amount of power, even if at a very low efficiency is impressive. Further refinement in especially the packing of the solar cell and the testing procedure can provide more accurate and better resolutes with only minor changes to this method.

ACKNOWLEDGMENTS

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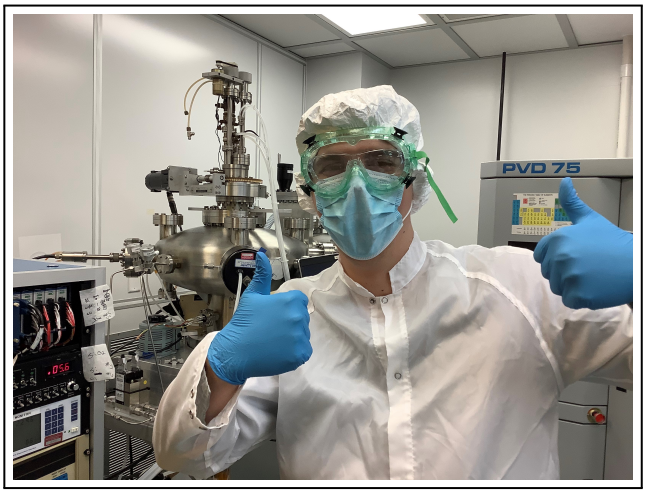

Figure 16. Nano-Scale Technology!

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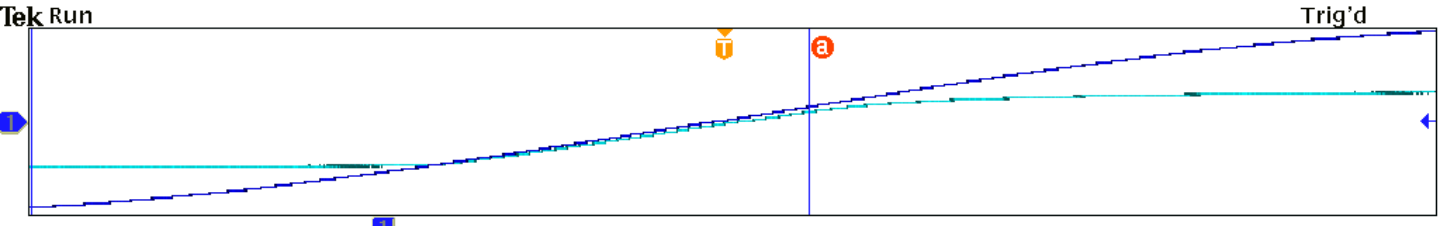
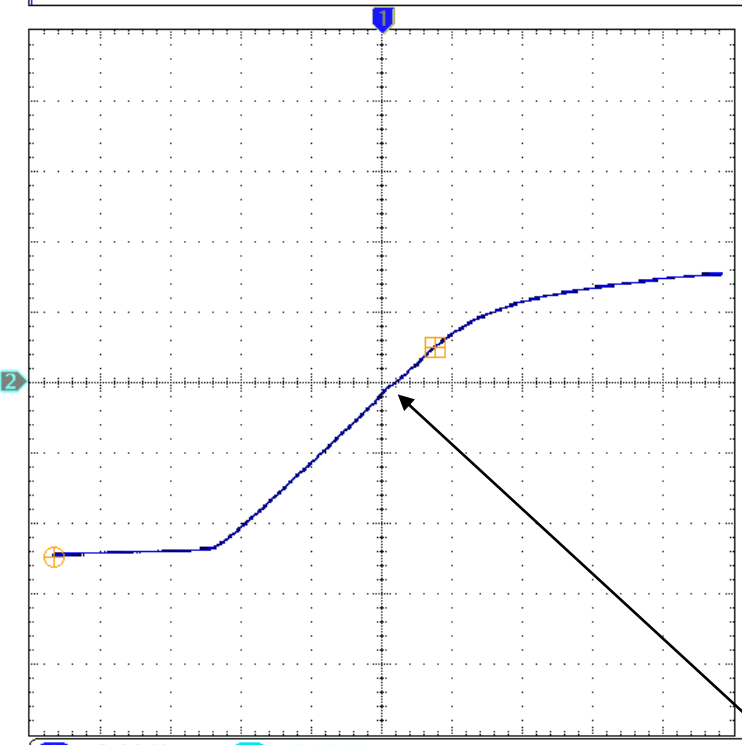
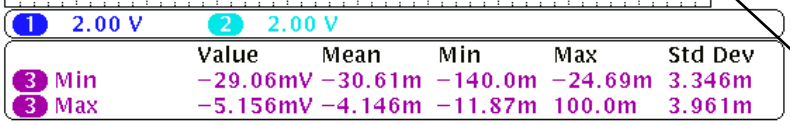
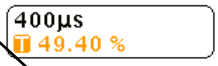
Transfer Function of the Solar Cell



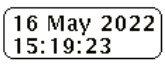


(1) (X) Versus (2) (Y)	a	b	Δ
	t: 240µs	−1.97ms	2.21ms
Rectangular	x: 1.47 V y: 942mV	−9.38 V −5.00 V	−10.8 V −5.94 V
Polar	r: 1.75 V θ: 32.6 °	10.6 V −152 °	12.4 V −151 °
Product	x×y: 1.39 VV	46.9 VV	64.5 VV
Ratio	y÷x: 641mV/V	533mV/V	548mV/V





	Value	Mean	Min	Max	Std Dev
3 Min	−29.06mV	−30.61m	−140.0m	−24.69m	3.346m
3 Max	−5.156mV	−4.146m	−11.87m	100.0m	3.961m



One can see where the diode crosses the axis is slightly off from the origin. This is due to the induced current from the solar cell